Energy Efficient Embedded Non-Volatile Memory & Logic Based on Ferroelectric Hf(Zr)O_2

3εFERRO is project for competitive, scalable FeRAM and logic-in-memory designs based on Si-compatible ferroelectric $Hf_xZr_{1-x}O_2$. The latest results on the materials optimization, logic design and integration into a 16 kbit test vehicle are highly encouraging.

Energy efficiency

The 3εFERRO consortium is researching energy efficient non-volatile memory and logic devices based on Si-compatible ferroelectric $HfZrO_2$ (HZO) to provide advanced embedded solutions for normally-off microcontroller units used in IoT. The consortium is a balanced mix of large technology development laboratories and academia in partnership with ST Microelectronics to address the complex issues associated with materials optimization, circuit design, device fabrication and integration.

At A Glance

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EC Contribution: € **3.99**m

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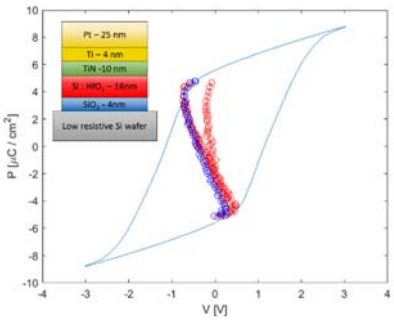
July 2019 - Special session HfO_2

Many fascinating presentations made in the joint ISAF-EMF-ICE special session on ferroelectric HfO_2, Lausanne, July 2019. More details here:

http://lausanne2019.org/pages/special-session-hfo2-based-ferroelectrics

Negative capacitance stabilized

The ongoing debate on the reality of negative capacitance (NC) has, to a large extent, been resolved by the recent work of 3εFERRO partner NamLab who demonstrated that adding an additional dielectric layer (Ta_2O_5) stabilizes NC in ferroelectric HZO [*Nature* **464**, 565 (2019)]. The experiments were done in a capacitance geometry, suitable for memory storage.

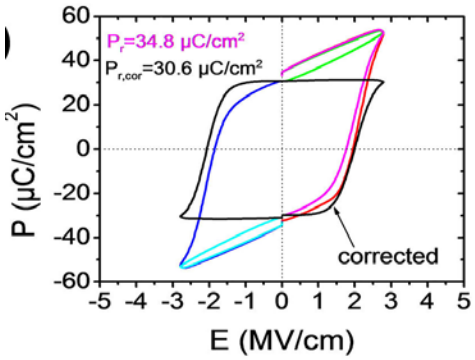


Work at the Ecole Polytechnique Fédérale de Lausanne has demonstrated negative capacitance in a FeFET like geometry using a $Si/SiO_2/Si:HfO_2/TiN$ structure. The NC shows up only at short (ns) pulses (and destroyed by dc). With faster pulses and thicker SiO_2 layers one can expect a stronger NC and lower level of leakage. Further enhancement of the NC may require more stable polarization without multidoman formation.

Ferroelectric HZO on Ge

Significant progress has been made on the growth of HZO on Ge substrates at the NCSRD in Athens for FeFET applications. At 225 °C, HZO crystallizes during deposition by molecular beam epitaxy and the ferroelectric orthorhombic phase is dominant.

Rapid thermal annealing (RTA) of the Ge/HZO/TiN/Ti/Pt metal-ferroelectric-semiconductor stack at 500°C yields a record remanent polarization of 30.6 μC/cm^2 and an endurance of 10^5 cycles at 2.3 MV/cm.



The low T crystallization annealing is compatible with low boron dopant activation annealing in Ge, opening up interesting perspectives for an optimized "gate last" FeFET process flow. The results have been published in *Appl. Phys. Lett.* **114**, 112901 (2019)

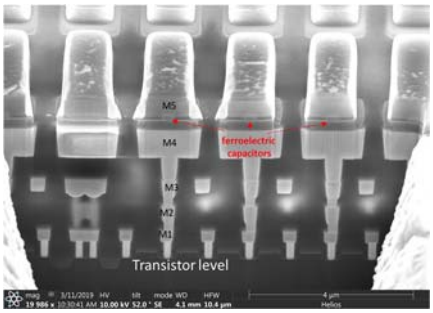
https://doi.org/10.1063/1.5090036

BEOL HZO integration with 130nm CMOS

The complete integration of FE layers above CMOS devices (1T-1C MAD200 wafers): the full integration approach of sub-μm² HZO-based capacitor was successfully achieved on a 16 kbit test vehicle produced at the CEA in Grenoble.

Wafers were processed by ST microelectronics with 130 nm node technology using the CEA MAD200v2 mask. After transistor fabrication, routing from M1 to M4 with standard process, bottom electrode was prepared at CEA. Wafers were then sent to NamLab for 10nm HZO growth and 10nm TiN capping. Following the specific cleaning procedure developed during the 1st year of the project, TiN top electrode was deposited in CEA. Then capacitors were patterned with DUV lithography. The capacitor size ranges from 300-550 nm diameter. The capacitors are encapsulated by silicon nitride and the process continues up to metal 5 (M5) level.

The figure shows a zoomed-out cross section of the 1T-1C full integration after M5 patterning. The first characterization results on the ferroelectric performance on the MAD200 test vehicle, originally designed for RRAM benchmarking are encouraging and full results will be reported soon.



System benchmarking platform

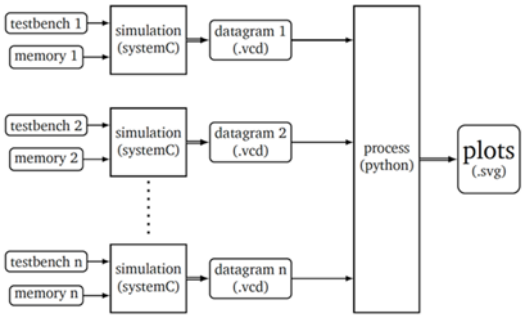
We have realized a system-level benchmarking platform at the Ecole Centrale Lyon, taking performance metrics from simulations operated at the device- and circuit-level.

The main evaluation tool is in SystemC, which enables direct interfacing to existing industry-standard benchmarks. This tool will guide design choices and provide a quantified feedback of the gains expected from normally-off computing and coarse-grain Logic-in-Memory (LiM).

"it is…possible to extrapolate these performance metrics to the system level"

Ian O'Connor
(Ecole Centrale Lyon)

Having such a feedback also enables co-optimization at the device level, with parameters such as transistor footprints being guided from system-level performance considerations.



The architecture of the platform mimics a memory circuit, whose parts reproduce energy and latency metrics observed in smaller memory bitcell arrays. This enables the comparison of realistic workload performance under normally-off, coarse-grained LiM.